REMARKS

Claim Rejection -- 35 U.S.C. 112

Claims 1-28 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner stated that it is misdescriptive to recite that the "feedback circuit" provides a feedback path between the first and second nodes.

While the applicants believe that their use of the term "feedback circuit" is appropriate, in the interest of expeditious prosecution of the application they have deleted .the word "feedback" from the claims.

Claim Rejection -- 35 U.S.C. 102(b)

Claims 1-28 were rejected under 35 U.S.C. 102(b) as being anticipated by Shin (U.S. Patent 5,874,844).

In the rejection of Claims 1-28 the Examiner stated that a first plurality of feedback circuits of Claim 1 of the present invention is represented in Shin by circuits 31, 33, 35. After careful study of the Shin reference, the Applicants respectfully disagree.

Applicants' invention is directed to a Schmitt trigger circuit with adjustable trip point voltages. As shown in applicants' Fig. 1 (and in Shin's Fig. 1), a prior art Schmitt trigger circuit implemented in CMOS technology comprises first, second, third and fourth MOS transistors TO, T1, T5, T4 connected in series and two additional MOS transistors T2, T3 that are connected as source followers. The gates of the two additional transistors are connected to node 30 between the second and third transistors. The source of transistor T2 is connected to node 50 between the first and second transistors; and the source of transistor T3 is connected to node 40 between the third and fourth transistors.

For this arrangement, the trip point voltages of the Schmitt trigger circuit are dependant on the power supply voltage VCC driving the circuit. However, if the value of VCC changes by a significant amount, resulting changes in the trip point voltages may no longer satisfy desired noise margins and other performance specifications.

Shin addresses this problem by providing in the circuit of Fig. 3 first and second voltage adjusting portions 35, 36 comprising several MOS transistors MP4, MP5, MP6;

MN4, MN5, MN6, that are connected in parallel across the source and drain of the source follower transistors MP3 and MN4 (sic). These transistors are controlled by A/D converters 31, 32 and inverter arrays 33, 34. At Col. 6, line 31 to Col. 7, line 30, Shin indicates that these transistors are selectively turned on or off to adjust the trigger voltage level depending on the digital values output from the A/D converters to the inverter arrays. Moreover, at Col. 5 lines 63-65 and Col. 6, line 17-18, Shin indicates that the time at which these transistors are switched on or off is the time of an input signal transition. And, proper operation of the source follower circuit would seem to require that all of the transistors connected across a source follower be off when the source follower is off. Thus, it is apparent that Shin provides a relatively complicated circuit to be able to adjust the trigger voltage level and that proper operation of this circuit imposes still other requirements.

Applicants, in contrast, have devised a simpler circuit for adjusting the trigger voltage of a Schmitt trigger circuit. In particular, as shown in applicants' Fig. 4, multiple, selectable circuits are provided between the second node 130 located between the second and third transistors T1, T5 and the first node 150 located between the first and second transistors T0, T1 and between the second node 130 and the third node 140 located between the third and fourth transistors T5, T4. Each such circuit includes a source follower illustratively implemented as an MOS transistor whose gate is connected to the second node and a selection switch illustratively implemented as another MOS transistor. Importantly, each circuit is connected to the second node; and the selection switches are operated so that only one circuit at a time can be supplying a signal to the first node and only one circuit can be supplying a signal to the third node.

Thus, applicants' circuit differs from Shin in that each circuit is connected to the second node and not just transistors MP3 and MN4 (sic) and only one circuit at a time can be connected from the second node to the first node and only one circuit at a time from the second node to the third node.

These differences are reflected in the claims. In particular, claim 1 requires both a first plurality of circuits selectively providing a first signal path between the second node and the first node and a second plurality of circuits selectively providing a second signal path between the second node and the third node. Shin discloses only one circuit connected between the second node and the first node and only one circuit connected between the

second node and the third node. Therefore, contrary to the Examiner's assertion, Shin does not anticipate applicants' claim 1 or claims 2-9 which are dependent thereon.

Claim 10 is similar to claim 1 in reciting a plurality of first circuits selectively providing a first signal path between the second node and the first node. Claim 10 and claims 11-14 which are dependent thereon are believed patentable for the same reason claim 1 is patentable.

Claim 15 is similar to claim 1 in reciting a plurality of second circuits for selectively providing a feedback path between the second node and the third node. Claim 15 and claims 16-19 which are dependent thereon are believed patentable for the same reason claim 1 is patentable.

Claim 20 recites a Schmitt trigger circuit having a first plurality of independent source follower circuits each having a different effect on the upper trip point level when selected and a second plurality of independent source follower circuits each having a different effect on the lower trip point level when selected. Further, the circuit receives control signal(s) for selecting one of the first plurality of circuits and one of the second plurality of circuits. Again, Shin discloses only one independent source follower circuit that affects the upper trip point level and only one independent source follower circuit that affects the lower trip point level; and, therefore, Shin does not anticipate claim 20 or claims 21-23 which are dependent thereon.

Claim 24 recites a Schmitt trigger circuit having a plurality of independent source follower circuits wherein the circuit receives a control signal for selecting one of the source follower circuits. Since Shin does not disclose a control signal for selecting a source follower circuit, Shin does not anticipate claim 24.

Claim 25 recites a method of providing an adjustable hysteresis characteristic in a Schmitt trigger circuit in which control signals are used to select one of a plurality of independent source follower circuits. Claim 25 and claim 26 which is dependent thereon are believed patentable for the same reason claim 24 is patentable.

In view of the foregoing, applicants believe that all of the claims are now in condition for allowance and respectfully request the Examiner to pass the subject application to issue. If for any reason the Examiner believes any of the claims are not in condition for allowance, he is encouraged to phone the undersigned at (650) 849-7777 so that any remaining issues

may be resolved.

Aside for the Petition for Extension of Time Fee, no additional fee is believed due for filing this response. However, if a fee is due, please charge such fee to Pennie & Edmonds LLP's Deposit Account No. 16-1150.

Respectfully submitted,

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APPENDIX A

Changes to the Claims

The rewritten claims were revised as follows:

1. (Amended) A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply [signal] node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a first plurality of [feedback] circuits for selectively providing a first [feedback] signal path between the second node and the first node, wherein each of said [feedback] circuits receives a control signal so that only one of the first plurality of [feedback] circuits provides the first [feedback] signal path at any one time; and

a second plurality of [feedback] circuits for selectively providing a [feedback] second signal path between the second node and the third node, wherein each of said [feedback] circuits receives a control signal so that only one of the second plurality of [feedback] circuits provides the second [feedback] signal path at any one time.

2. (Amended) The circuit of claim 1 wherein:

each [feedback] circuit in the first plurality of [feedback] circuits comprises a first [feedback] transistor and a second [feedback] transistor, the first [feedback] transistor having a control terminal coupled to the second node and the first [feedback] transistor being coupled between the power supply signal node and the second [feedback] transistor, the second [feedback] transistor having a control terminal for receiving the control signal provided to said [feedback] circuit and the second [feedback] transistor being coupled between the first [feedback] transistor and the first node; and

each [feedback] circuit in the second plurality of [feedback] circuits comprises a first [feedback] transistor and a second [feedback] transistor, the first [feedback] transistor having

a control terminal coupled to the second node and the first [feedback] transistor being coupled between the reference node and the second [feedback] transistor, the second [feedback] transistor having a control terminal for receiving the control signal provided to said [feedback] circuit and the second [feedback] transistor being coupled between the first [feedback] transistor and the third node.

3. (Amended) The circuit of claim 2 wherein:

the [feedback] transistors in each [feedback] circuit in the first plurality of [feedback] circuits have a combined conductivity that is different from the combined conductivity of the [feedback] transistors in any other [feedback] circuit in the first plurality of [feedback] circuits; and

the [feedback] transistors in each [feedback] circuit in the second plurality of [feedback] circuits have a combined conductivity that is different from the combined conductivity of the [feedback] transistors in any other [feedback] circuit in the second plurality of [feedback] circuits.

4. (Amended) The circuit of claim 2 wherein:

the first transistor, the second transistor, and the [feedback] transistors in each [feedback] circuit in the first plurality of [feedback] circuits are of a first type; and

the third transistor, the fourth transistor, and the [feedback] transistors in each [feedback] circuit in the second plurality of [feedback] circuits are of a second type.

6. (Amended) The circuit of claim 5 wherein:

the first [feedback] transistor in each [feedback] circuit in the first plurality of [feedback] circuits has a different threshold voltage magnitude from that of the first [feedback] transistor in any other [feedback] circuit in the first plurality of [feedback] circuits; and

the first [feedback] transistor in each [feedback] circuit in the second plurality of [feedback] circuits has a different threshold voltage magnitude from that of the first [feedback] transistor in any other [feedback] circuit in the second plurality of [feedback] circuits.

7. (Amended) The circuit of claim 4 wherein

a source terminal of the first transistor is coupled to the reference node and a drain terminal of the first transistor is coupled to the first node;

a source terminal of the second transistor is coupled to the first node and a drain terminal of the second transistor is coupled to the second node;

a drain terminal of the third transistor is coupled to the second node and a source terminal of the third transistor is coupled to the third node;

a drain terminal of the fourth transistor is coupled to the third node and a source terminal of the fourth transistor is coupled to the power supply signal node;

in each [feedback] circuit in the first plurality of [feedback] circuits, a drain terminal of the first [feedback] transistor is coupled to the power supply signal node, a source terminal of the first [feedback] transistor is coupled to a drain terminal of the second [feedback] transistor, and a source terminal of the second [feedback] transistor is coupled to the first node; and

in each [feedback] circuit in the second plurality of [feedback] circuits, a drain terminal of the first [feedback] transistor is coupled to the reference node, a source terminal of the first [feedback] transistor is coupled to a drain terminal of the second [feedback] transistor, and a source terminal of the second [feedback] transistor is coupled to the third node.

8. (Amended) The circuit of claim 1 wherein the first and second plurality of [feedback] circuits each consists of first and second [feedback] circuits, wherein the first [feedback] circuits in each plurality of [feedback] circuits receive a common control signal and the second [feedback] circuits in each plurality of [feedback] circuits receive a complementary version of said common control signal.

9. (Amended) The circuit of claim 1 wherein the control signals provided to each [feedback] circuit are programmable settings.

10. (Amended) A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply [signal] node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a plurality of first [feedback] circuits for selectively providing a first [feedback] signal path between the second node and the first node, wherein each of the first [feedback] circuits receives a control signal so that only one of the first [feedback] circuits provides the first [feedback] signal path at any one time; and

a second [feedback] circuit for providing a second [feedback] signal path between the second node and the third node.

11. (Amended) The circuit of claim 10 wherein:

each first [feedback] circuit comprises a first [feedback] transistor and a second [feedback] transistor, the first [feedback] transistor having a control terminal coupled to the second node and the first [feedback] transistor being coupled between the power supply signal node and the second [feedback] transistor, the second [feedback] transistor having a control terminal for receiving the control signal provided to said [feedback] circuit and the second [feedback] transistor being coupled between the first [feedback] transistor and the first node; and

the second [feedback] circuit comprises a [feedback] transistor having a control terminal coupled to the second node and said [feedback] transistor being coupled between the reference node and the third node.

12. (Amended) The circuit of claim 11 wherein:

the [feedback] transistors in each of the plurality of first [feedback] circuits have a combined conductivity that is different from the combined conductivity of the [feedback] transistors in any other first [feedback] circuit.

13. (Amended) The circuit of claim 11 wherein:

the first transistor, the second transistor, and the [feedback] transistors in each of the plurality of first [feedback] circuits are of a first type; and

the third transistor, the fourth transistor, and the [feedback] transistor in the second [feedback] circuit are of a second type.

15. (Amended) A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply [signal] node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a first [feedback] circuit for providing a first [feedback] signal path between the second node and the first node; and

a plurality of second [feedback] circuits for selectively providing a second [feedback] signal path between the second node and the third node, wherein each of the second [feedback] circuits receives a control signal so that only one of the second [feedback] circuits provides the second [feedback] signal path at any one time.

16. (Amended) The circuit of claim 15 wherein:

the first [feedback] circuit comprises a [feedback] transistor having a control terminal coupled to the second node and the [feedback] transistor being coupled between the power supply [signal] node and the first node; and

each [feedback] circuit in the plurality of second [feedback] circuits comprises a first [feedback] transistor and a second [feedback] transistor, the first [feedback] transistor having a control terminal coupled to the second node and the first [feedback] transistor being coupled between the reference node and the second [feedback] transistor, the second [feedback] transistor having a control terminal for receiving the control signal provided to said [feedback] circuit and the second [feedback] transistor being coupled between the first [feedback] transistor and the third node.

17. (Amended) The circuit of claim 16 wherein:

the [feedback] transistors in each of the plurality of second [feedback] circuits have a combined conductivity that is different from the combined conductivity of the [feedback] transistors in any other second [feedback] circuit.

18. (Amended) The circuit of claim 16 wherein:

the first transistor, the second transistor, and the [feedback] transistor in the first [feedback] circuit are of a first type; and

the third transistor, the fourth transistor, and the [feedback] transistors in each of the plurality of second [feedback] circuits are of a second type.

20. (Amended) A Schmitt trigger circuit for receiving an input signal and outputting a signal in accordance with a voltage transfer characteristic having an upper trip point level and a lower trip point level, the circuit comprising a first plurality of independent [feedback] source follower circuits, each providing a different effect on the upper trip point level when selected, and a second plurality of independent [feedback] source follower circuits, each providing a different effect on the lower trip point level when selected, and wherein the Schmitt trigger circuit receives one or more control signals for selecting one [feedback] circuit in the first plurality of [feedback] circuits and one [feedback] circuit in the second plurality of [feedback] circuits.

21. (Amended) The circuit of claim 20 wherein the [feedback] circuits in the first plurality of [feedback] source follower circuits comprise n-channel metal oxide semiconductor field-effect transistors, and the [feedback] source follower circuits in the second plurality of [feedback] circuits comprise p-channel metal oxide semiconductor field-effect transistors.

22. (Amended) The circuit of claim 21 wherein:

the transistors in each [feedback] circuit in the first plurality of [feedback] source follower circuits have a combined conductivity that is different from the combined conductivity of the [feedback] transistors in any other [feedback] circuit in the first plurality of [feedback] source follower circuits; and

the transistors in each [feedback] circuit in the second plurality of [feedback] source follower circuits have a combined conductivity that is different from the combined conductivity of the [feedback] transistors in any other [feedback] circuit in the second plurality of [feedback] source follower circuits.

24. (Amended) A Schmitt trigger circuit for receiving an input signal and outputting a signal in accordance with a voltage transfer characteristic having an upper trip point level and a lower trip point level, the circuit comprising a plurality of independent [feedback] source follower circuits each providing, when selected, a different effect on one of the upper trip point level and the lower trip point level, and wherein the Schmitt trigger circuit receives one or more control signals for selecting one [feedback] source follower circuit in the plurality of [feedback] source follower circuits.

25. (Amended) A method of providing an adjustable hysteresis characteristic in a Schmitt trigger circuit comprising:

providing one or more control signals to the Schmitt trigger circuit; and

in response to the one or more control signals, selecting one of a first plurality of independent [feedback] source follower circuits to provide a first desired [feedback] signal path in the Schmitt trigger circuit.

26. (Amended) The method of claim 25 further comprising:

in response to the one or more control signals, selecting one of a second plurality of independent [feedback] source follower circuits to provide a second desired [feedback] signal path in the Schmitt trigger circuit.